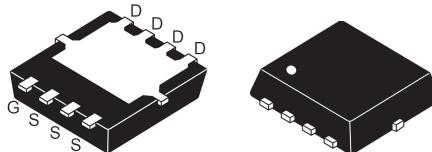
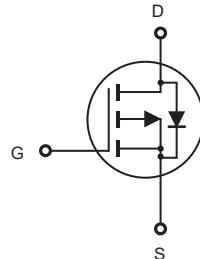


## P-Channel Enhancement Mode Field Effect Transistor

### FEATURES

- -30V, -37A,  $R_{DS(ON)} = 10m\Omega$  @  $V_{GS} = -10V$ .
- $R_{DS(ON)} = 15m\Omega$  @  $V_{GS} = -4.5V$ .
- Super High dense cell design for extremely low  $R_{DS(ON)}$ .
- High power and current handing capability.
- RoHS compliant.



P-PAK 3X3

### ABSOLUTE MAXIMUM RATINGS $T_A = 25^\circ C$ unless otherwise noted

Parameter	Symbol	Limit	Units
Drain-Source Voltage	$V_{DS}$	-30	V
Gate-Source Voltage	$V_{GS}$	$\pm 20$	V
Drain Current-Continuous	$I_D @ R_{\theta JC}$	$T_C = 25^\circ C$	-37
		$T_C = 100^\circ C$	-23
	$I_D @ R_{\theta JA}$	$T_A = 25^\circ C$	-11
		$T_A = 100^\circ C$	-7
Drain Current-Pulsed <sup>a</sup>	$I_{DM} @ R_{\theta JC}$	$T_C = 25^\circ C$	-148
	$I_{DM} @ R_{\theta JA}$	$T_A = 25^\circ C$	-44
Maximum Power Dissipation	$P_D @ R_{\theta JC}$	$T_C = 25^\circ C$	25
	$P_D @ R_{\theta JA}$	$T_A = 25^\circ C$	2.5
Operating and Store Temperature Range	$T_J, T_{Stg}$	-55 to 150	$^\circ C$

### Thermal Characteristics

Parameter	Symbol	Limit	Units
Thermal Resistance, Junction-to-Case <sup>b</sup>	$R_{\theta JC}$	5	$^\circ C/W$
Thermal Resistance, Junction-to-Ambient <sup>b</sup>	$R_{\theta JA}$	50	$^\circ C/W$



# CEZC3P07A

## Electrical Characteristics $T_C = 25^\circ\text{C}$ unless otherwise noted

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
<b>Off Characteristics</b>						
Drain-Source Breakdown Voltage	$\text{BV}_{\text{DSS}}$	$V_{\text{GS}} = 0\text{V}, I_D = -250\mu\text{A}$	-30			V
Zero Gate Voltage Drain Current	$I_{\text{DSS}}$	$V_{\text{DS}} = -30\text{V}, V_{\text{GS}} = 0\text{V}$			-1	$\mu\text{A}$
Gate Body Leakage Current, Forward	$I_{\text{GSSF}}$	$V_{\text{GS}} = 20\text{V}, V_{\text{DS}} = 0\text{V}$			100	nA
Gate Body Leakage Current, Reverse	$I_{\text{GSSR}}$	$V_{\text{GS}} = -20\text{V}, V_{\text{DS}} = 0\text{V}$			-100	nA
<b>On Characteristics<sup>c</sup></b>						
Gate Threshold Voltage	$V_{\text{GS}(\text{th})}$	$V_{\text{GS}} = V_{\text{DS}}, I_D = -250\mu\text{A}$	-1		-3	V
Static Drain-Source On-Resistance	$R_{\text{DS}(\text{on})}$	$V_{\text{GS}} = -10\text{V}, I_D = -10\text{A}$		8	10	$\text{m}\Omega$
		$V_{\text{GS}} = -4.5\text{V}, I_D = -5\text{A}$		11.5	15	$\text{m}\Omega$
<b>Dynamic Characteristics<sup>d</sup></b>						
Input Capacitance	$C_{\text{iss}}$	$V_{\text{DS}} = -15\text{V}, V_{\text{GS}} = 0\text{V}, f = 1.0 \text{ MHz}$		2020		pF
Output Capacitance	$C_{\text{oss}}$			390		pF
Reverse Transfer Capacitance	$C_{\text{rss}}$			170		pF
<b>Switching Characteristics<sup>d</sup></b>						
Turn-On Delay Time	$t_{\text{d}(\text{on})}$	$V_{\text{DD}} = -15\text{V}, I_D = -10\text{A}, V_{\text{GS}} = -10\text{V}, R_{\text{GEN}} = 6\Omega$		18		ns
Turn-On Rise Time	$t_r$			8		ns
Turn-Off Delay Time	$t_{\text{d}(\text{off})}$			108		ns
Turn-Off Fall Time	$t_f$			31		ns
Total Gate Charge	$Q_g$	$V_{\text{DS}} = -15\text{V}, I_D = -10\text{A}, V_{\text{GS}} = -5\text{V}$		24		nC
Gate-Source Charge	$Q_{\text{gs}}$			7		nC
Gate-Drain Charge	$Q_{\text{gd}}$			10		nC
<b>Drain-Source Diode Characteristics and Maximum Ratings</b>						
Drain-Source Diode Forward Current	$I_S$				-2.5	A
Drain-Source Diode Forward Voltage <sup>c</sup>	$V_{\text{SD}}$	$V_{\text{GS}} = 0\text{V}, I_S = -1\text{A}$			-1	V

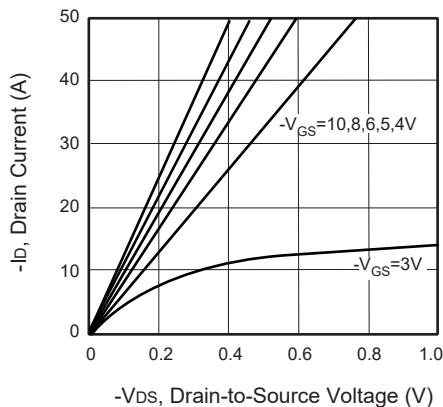
**Notes :**

a Repetitive Rating : Pulse width limited by maximum junction temperature

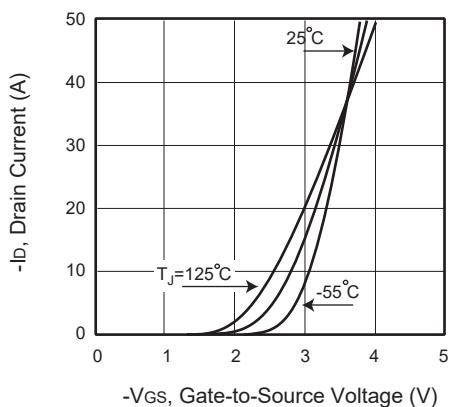
b.Surface Mounted on FR4 Board,  $t \leq 10$  sec.

c.Pulse Test : Pulse Width  $\leq 300\mu\text{s}$ , Duty Cycle  $\leq 2\%$ .

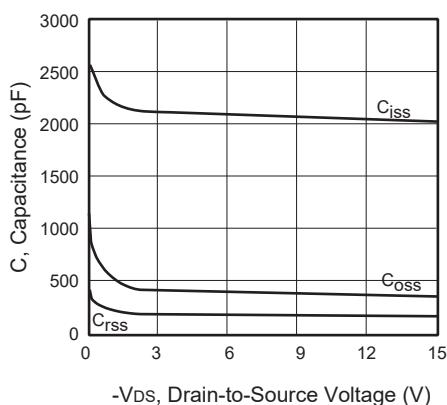
d.Guaranteed by design, not subject to production testing.



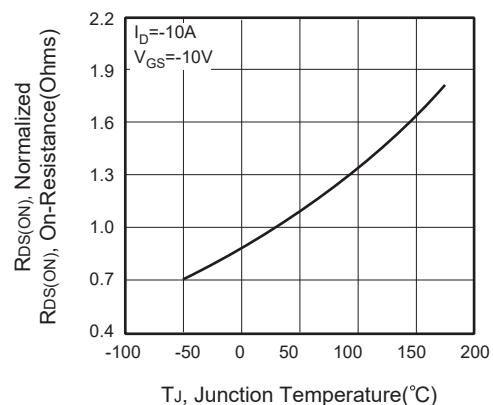
**Figure 1. Output Characteristics**



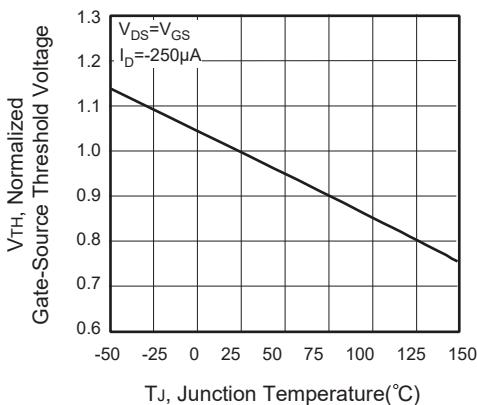
**Figure 2. Transfer Characteristics**



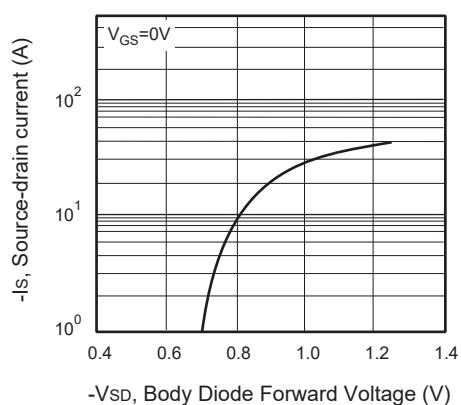
**Figure 3. Capacitance**



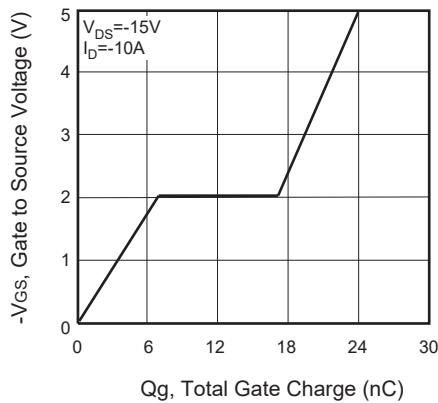
**Figure 4. On-Resistance Variation with Temperature**



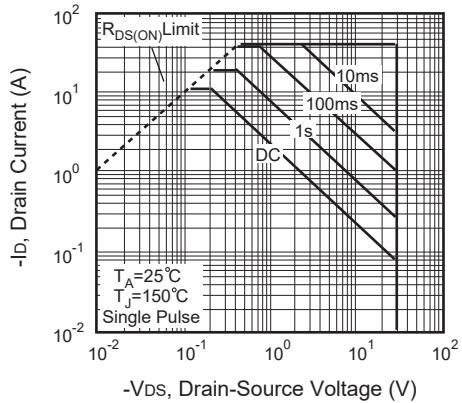
**Figure 5. Gate Threshold Variation with Temperature**



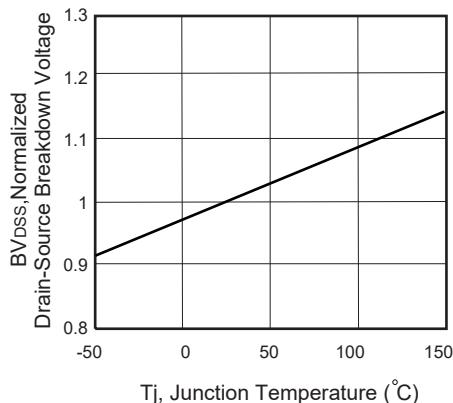
**Figure 6. Body Diode Forward Voltage Variation with Source Current**



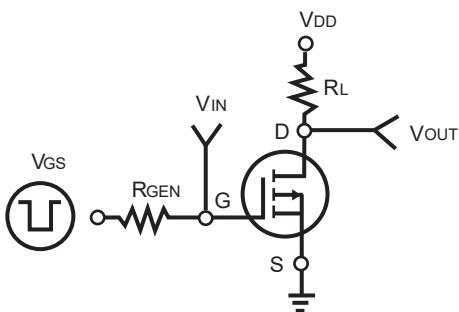
**Figure 7. Gate Charge**



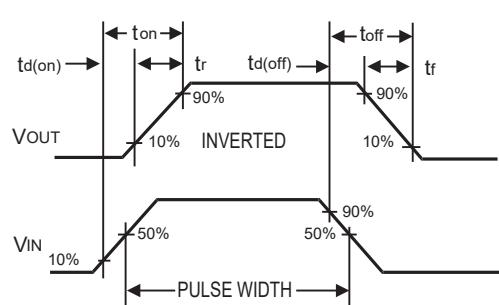
**Figure 8. Maximum Safe Operating Area**



**Figure 9. Breakdown Voltage Variation VS Temperature**



**Figure 10. Switching Test Circuit**



**Figure 11. Switching Waveforms**

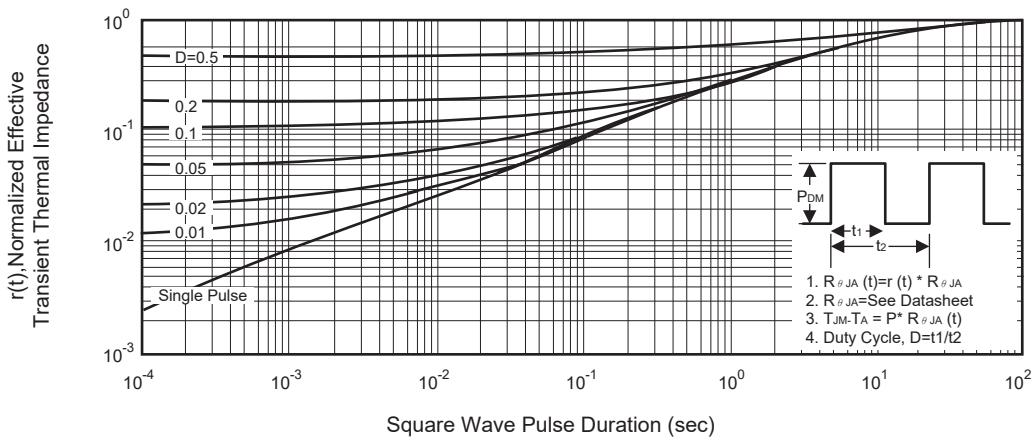
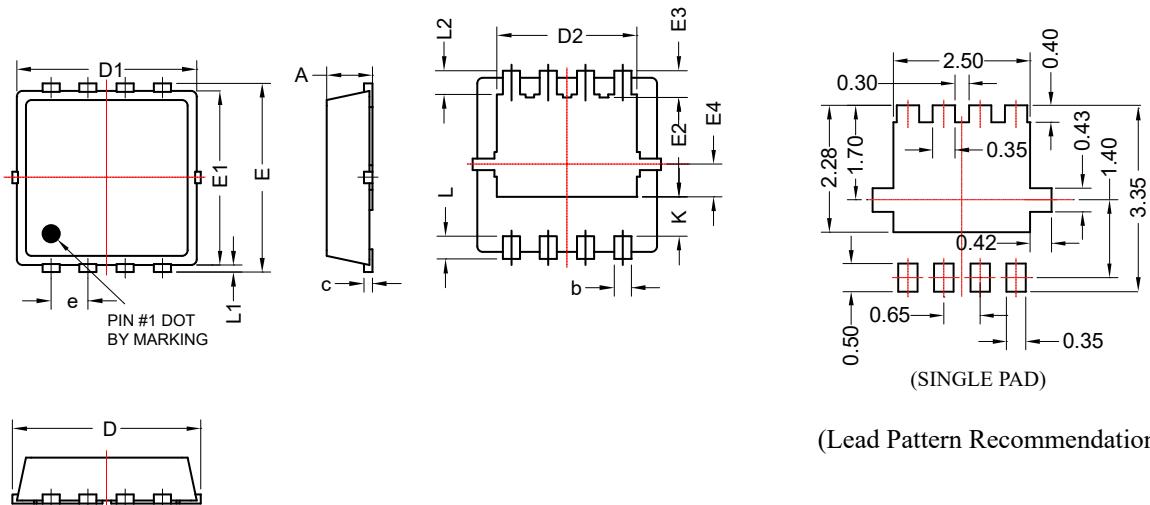


Figure 12. Normalized Thermal Transient Impedance Curve

## P-PAK 3X3 產品外觀尺寸圖 (Product Outline Dimension)

## SINGLE PAD 尺寸圖



SYMBOLS	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	0.7	0.85	0.028	0.033
b	0.20	0.40	0.008	0.016
c	0.10	0.25	0.004	0.010
D	3.15	3.45	0.124	0.136
D1	3.00	3.25	0.118	0.128
D2	2.29	2.65	0.090	0.104
E	3.15	3.45	0.124	0.136
E1	2.90	3.20	0.114	0.126
E2	1.54	1.94	0.061	0.076
E3	0.28	0.65	0.011	0.026
E4	0.37	0.77	0.015	0.030
e	0.65(BSC)		0.026(BSC)	
K	0.50	0.89	0.02	0.035
L	0.30	0.50	0.012	0.020
L1	0.06	0.20	0.002	0.008
L2	0.27	0.57	0.011	0.022